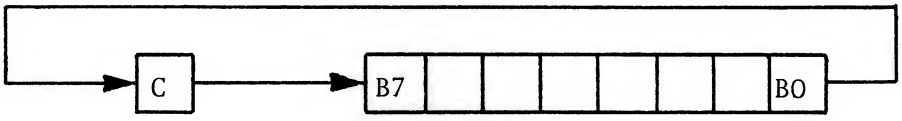
MCS650X FAMILY CIRCUIT MODIFICATIONS

1. Since introduction of the MCS650X Family numerous customers have requested the addition of the ROR Instruction. This instruction is now being added to all MCS650X processors. The addressing modes will be Absolute (6 cycles, 3 bytes); Zero Page (5, 2); Accumulator (2, 1); Zero Page, X (6, 2); Absolute, X (7, 3). The implementation of ROR involves shifting all addressed locations one bit to the right with the carry bit shifted into Bit location 7 and Bit location 0 shifted into the carry position.



2. An additional modification is being made to the Branch, Ready circuitry. The present MCS650X processors do not execute the branch instructions correctly when the ready signal is used in the Single Cycle Mode if the low order effective address is FF without crossing page boundaries. For clarification the following program is executed, in both Single Cycle Mode and Single Instruction Mode.

Sample Program

Memory	Contents	
F5	18	CLC
F6	90	BCC
F7	07	offset
F8	A9	LDAIMM

Sample Program Execution

Single Cycle

ABH	ABL	DB	SYNC	
XX	F5	18	1	CLC
XX	F6	90	0	
XX	F6	90	1	BCC
XX	F7	07	0	
XX	F8	09	0	
XX	FF	(XX+1,FF)	1	

Single Instruction

ABH	ABL	DB	SYNC
XX	F5	18	1
XX	F6	90	1
XX	FF	(XXFF)	1

Note that in the Single Cycle Mode the ADH of the branch destination is incremented while in the Single Instruction Mode the branch is properly executed. The only time this occurs is when the ADL of the branch destination is FF and then only during Single Cycle with no page crossing; hence, the probability of this occurring in normal application is remote.

Availability - MCS650X microprocessors incorporating the above changes will be available in sample quantities in April with production deliveries beginning in May. Pricing for these versions of the microprocessor will be identical to the product currently being shipped.

CLOCK GENERATOR INFORMATION

Initial characterization of the MCS650X clock generator circuit has provided us with sufficient information to update the clock generator information found in our manuals and data sheets. The following discussion provides the user with information needed to obtain best performance for the time base generation scheme chosen.

Generally one would consider the following when designing systems with the MCS650X.

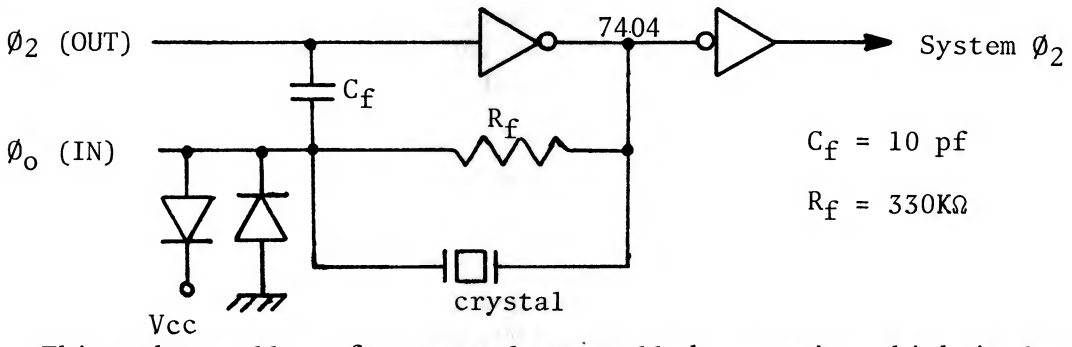
1. Which clock scheme is the best?

   There is no <u>one</u> answer, however depending on the system there is <u>one</u> best way

   A. TTL generated clock - drive $\emptyset_o$ (IN) with a TTL level clock, it doesn't require a high level clock; merely V_{OL} = .4V, V_{OH} = 2.4V. Buffer $\emptyset_2$ (OUT) for use as system $\emptyset_2$ clock. This scheme allows maximum control of all clock variables (i.e. symmetry, frequency, frequency variation from system to system).

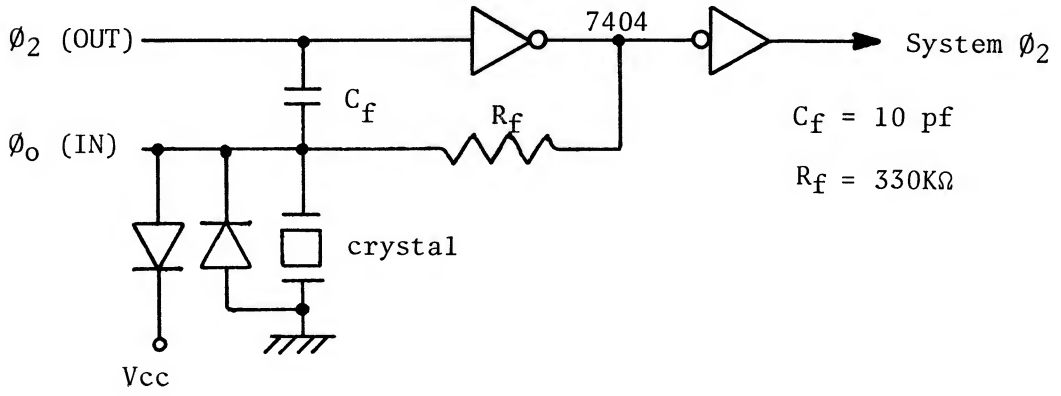
      In the following discussion, reference will be made to $\emptyset_o$ (IN) and $\emptyset_2$ (OUT). The applicable pin numbers on the various MCS650X processors are found in the manuals or data sheets. The diodes (IN914's) are for the purposes of clamping the clock swings near ground and near V_{DD} and may not be required in all crystal applications.

   B. Series Mode Crystal Controlled



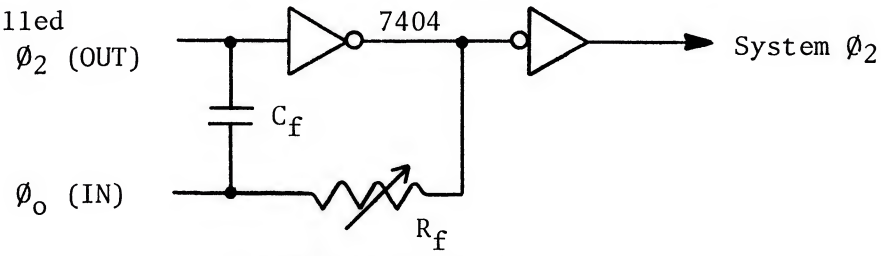
   This scheme allows for crystal controlled operation which is least sensitive to crystal parameters and feedback circuit variables. Because the crystal is <u>in</u> the feedback path and not shunting as the parallel mode crystal controlled scheme, the <u>serial mode is most reliable from a start-up standpoint.</u>

   C. Parallel Mode Crystal Controlled



This scheme should be used when the symmetry is more desirable than the Serial Mode crystal controlled scheme symmetry. This scheme is most sensitive to feedback parameters as related to start-up. By varying the feedback resistor an appropriate combination can be found for the crystal chosen.

D. RC Controlled



This scheme is recommended for those systems which do not require symmetry control, frequency variation control from system to system without manual adjustment, and systems where noise has been minimized.

Because of the ease of use of this scheme it is recommended for those systems which are in development, used as a microprocessor learning vehicle or in general systems in which noise on the clock circuit has been carefully handled (i.e. clean supply to microprocessor and clock buffers, isolate ϕ_2 (OUT) and ϕ_2 (IN) from stray system noise).

For frequency of operation around 1 MH_z a value of 10K to 50K should be used with C_f = 10 pf. To decrease noise sensitivity increase C_f and decrease R_f. Also a shunting capacitor to ground from ϕ_2 (OUT) the value of which should be the same range as C_f, will help to decrease sensitivity to noise in the system.

2. What is the maximum clock loading?

One standard TTL Load and 30 pf

If the clock outputs (ϕ_1 (OUT) and ϕ_2 (OUT)) are loaded, there is the possibility of causing overlap, but this has no effect on the internal clocks on the microprocessor. The system designer should therefore be careful if non-overlapping system clocks are necessary such that the microprocessor can function properly with overlapped clocks but system problems can develop.

3. How can clock ringing be prevented?

A. Eliminate noise from ϕ_o (IN). The clock generator on the MCS650X will react to frequencies as high as 20 MH_z, therefore it will also respond to noise.

B. Be sure the negative feedback (R_f) occurs after the positive feedback (C_f). This is most easily accomplished by tapping off the negative feedback after the positive feedback (note the inverter delay in the RC controlled schematic).

4. What are the typical clock widths and separations for TTL clock levels in? See graph #1.

5. What are typical frequencies for various RC combinations?

The RC values listed below provide the approximate operating frequencies listed. It is recommended that variable resistor pots be used if accuracy in the value of the operating frequency is required.

Typical Frequency	R_f	C_f
.5 MH_z	42K	10 pf
1.0 MH_z	17K	10 pf
2.0 MH_z*	6K	10 pf

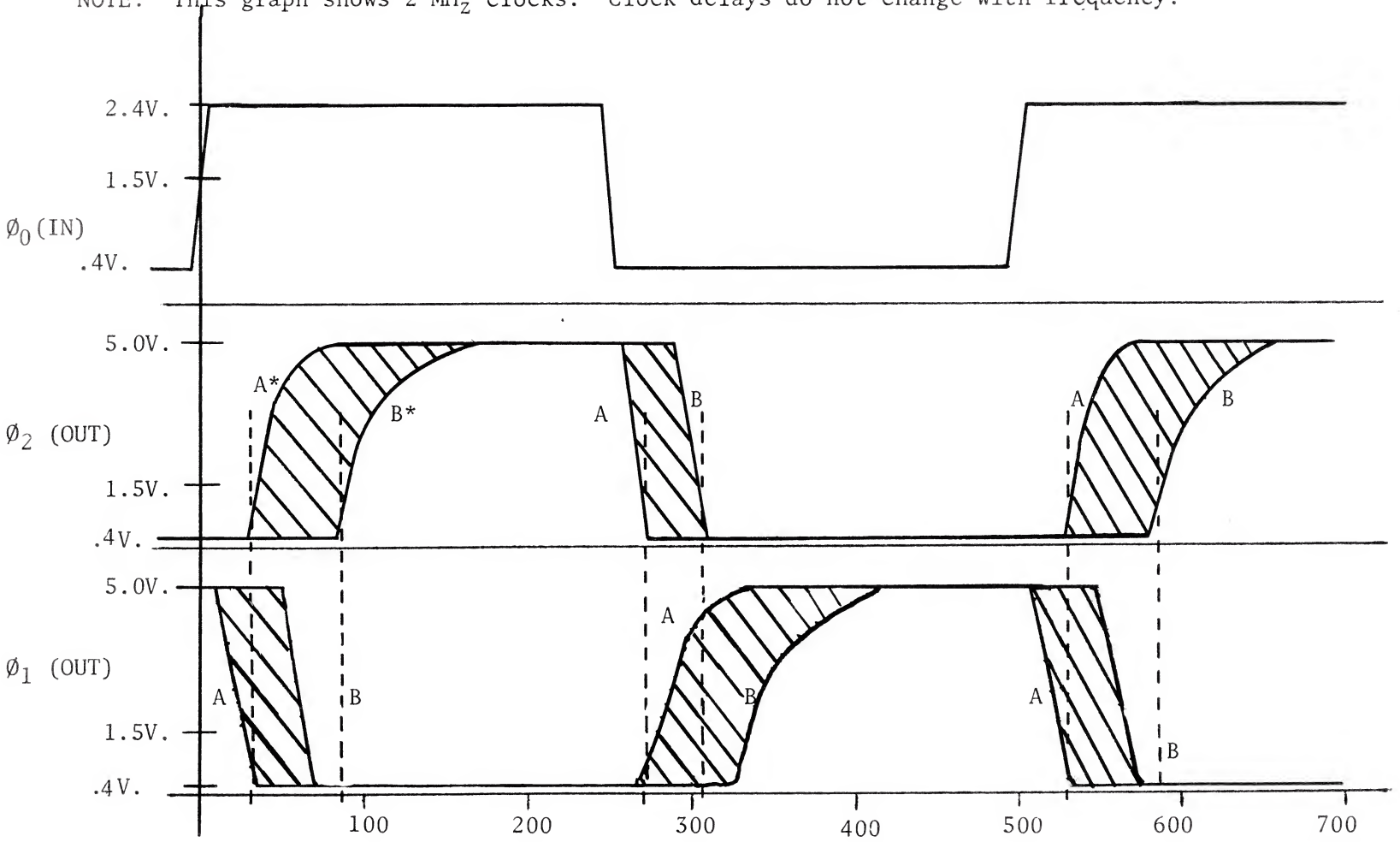
*Applies to product guaranteed at 2 MH_z operation.

NOTE: It should be understood that for maximum confidence in control of symmetry of the system clocks, it is recommended the TTL level $\emptyset_o$ (IN) be used. This can be generated from, for example a divide down from a high frequency crystal. In any case maximum pulse width control is formed with these inputs to $\emptyset_o$ (IN) in which the user has maximum control of the edges.

GRAPH #1

CLOCK PHASE RELATIONSHIPS

NOTE: This graph shows 2 MH_Z clocks. Clock delays do not change with frequency.



*Typical process related values. Edges marked "A" would correspond to part "A"
Edges marked "B" would correspond to part "B"

PRECAUTIONARY HANDLING PROCEDURES

FOR "MOS" TYPE PRODUCTS

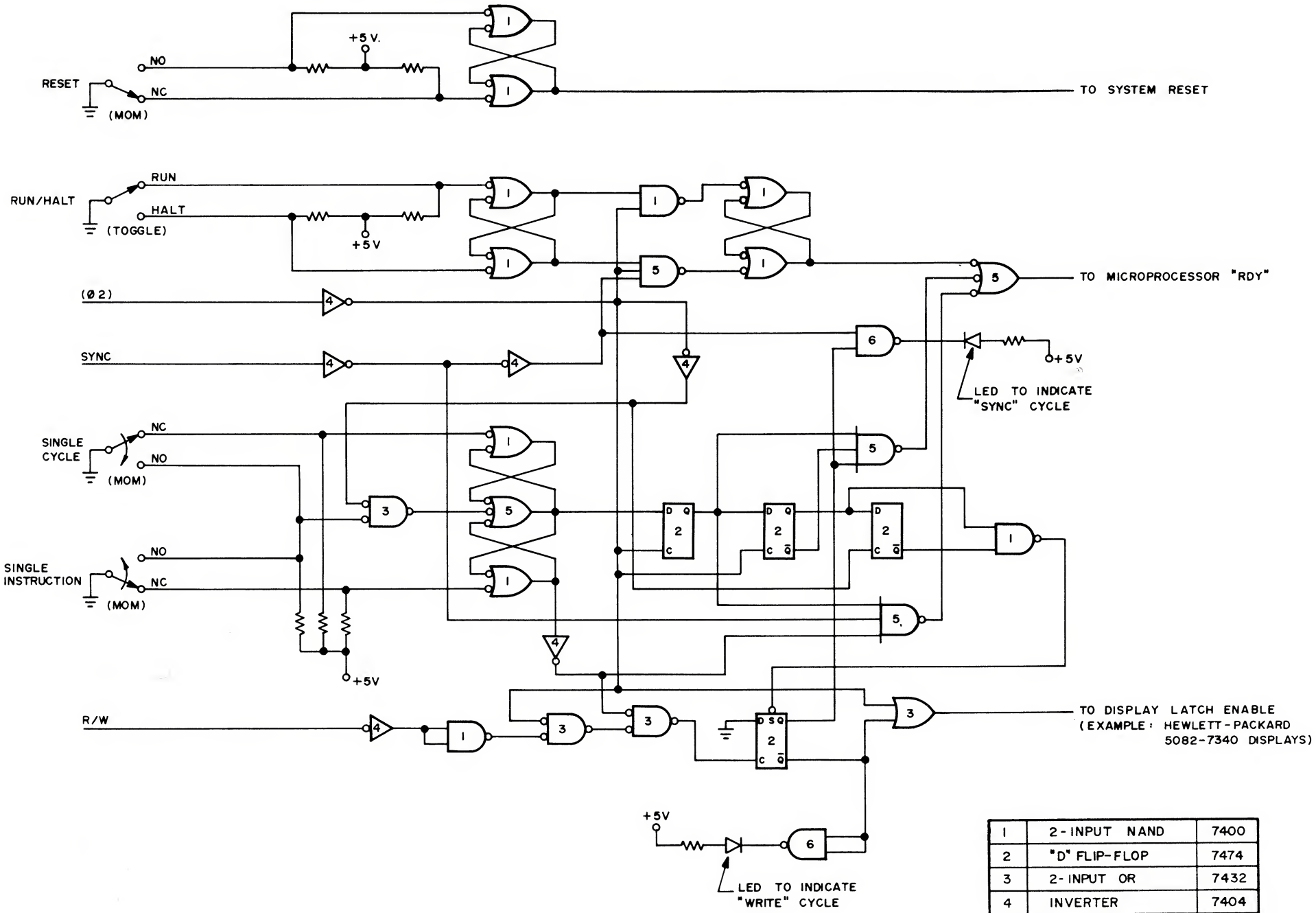
The MCS6500 Product Line has been designed with protective circuitry to guard against static charge damage on the inputs. However, normal precautions should be taken whenever possible to prevent exposure to environments of potential static charge. The following guidelines are recommended in handling the "MOS" type products and should be used whenever possible:

* Keep devices in the conductive shipping carrier until used.

* Perform work involving the "MOS" devices on a conductive surface where possible.

* In board assembly, place the "MOS" devices on the boards as late in the assembly cycle as possible. For low volume applications we recommend usage of a plug-in socket for the devices.

* Do not place the "MOS" device into position with power on. Always power up after the device is in place in the board assembly.



1	2-INPUT NAND	7400
2	"D" FLIP-FLOP	7474
3	2-INPUT OR	7432
4	INVERTER	7404
5	3-INPUT NAND	7410
6	2-INPUT NAND OPEN COLLECTOR	7403

SINGLE CYCLE / SINGLE INSTRUCTION

CONTROL LOGIC

SALES OFFICES AND REPRESENTATIVES FOR MOS TECHNOLOGY, INC.

EASTERN REGION

REGIONAL DIRECTOR

William Whitehead
MOS TECHNOLOGY, INC.
410 Jericho Turnpike, Suite 312
Jericho, N.Y. 11753
516-822-4240

NEW ENGLAND STATES

The Orion Group
P. O. Box 248
Mont Vernon, N.H. 03057
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Norvell Associates, Inc.
P. O. Box 20279
10210 Monroe Drive
Dallas, Texas 75220
214-350-6771

WESTERN REGION

REGIONAL DIRECTOR

Jack Turk
MOS TECHNOLOGY, INC.
2172 Dupont Drive
Patio Bldg.
Irvine, CA. 92715
714-833-1600

APPLICATIONS MANAGER

Petr Sehnal
MOS TECHNOLOGY, INC.
22300 Foothill Blvd.
Hayward, CA. 94541
415-881-8080

ARIZONA, NEW MEXICO

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W. W. Posey Company, Inc.
895 Sherwood Ave.
Los Altos, CA. 94022
415-948-7771

SALES OFFICE AND FOREIGN REPRESENTATIVES

EUROPEAN SALES DIRECTOR

Mr. Gerold G. Wiese
MOS TECHNOLOGY, INC.
6382 Friedrichstdorf 2 (F. Frankfurt)
Otto-Hahn-Strasse 40
W. Germany
(06175) 1510, 1519

HONG KONG AND TAIWAN

Mr. Lyle Ronalds
SOLID STATE INTERNATIONAL
Daily House Suite 48
35-39 Haiphong Road
Kowloon, Hong Kong
China

JAPAN AND ITS TERRITORIES

Nihon Teksel Co., Ltd.
13-14 Sakuragaoka-Machi
Shibuya-Ku, Tokyo
Japan
(03) 461-5121

INDIA

Mr. Dinish C. Gupta
Superior Electronics
E13 Dattaguru Society
Deonarpada Road
Bombay 400 088 India

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